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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,463	11/29/2001	Matthew John Fairhurst	TUC920010104US1	5676

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EXAMINER

BONURA, TIMOTHY M

ART UNIT

PAPER NUMBER

2114

DATE MAILED: 08/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/998,463

Applicant(s)

FAIRHURST ET AL.

Examiner

Tim Bonura

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 November 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-54 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4,7,9,12,13,16,18-22,25,27,30,31,34,36-40,43,45,48,49,52 and 54 is/are rejected.
- 7) ☒ Claim(s) 5,6,8,10,11,14,15,17,23,24,26,28,29,32,33,35,41,42,44,46,47,50,51 and 53 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 November 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 7, 9, 12, 13, 16, 18-22, 25, 27, 30, 31, 34, 36-40, 43, 45, 48-49, 52, and 54 are rejected under 35 U.S.C. 102(b) as being anticipated by Powers, et al, U.S. Patent Number 5,212,785.

3. Regarding claim 1:

a. Regarding the limitation of “detecting an error in a system including a first adaptor, wherein the first adaptor is capable of communicating on the storage network after the error is detected,” Powers discloses a system with a plurality of memory devices and components for controlling data flow with failure handling. (Lines 50-55 of Column 1).

b. Regarding the limitation of “determining whether the first adaptor is designated a master of the storage network after the error is,” Powers discloses a system wherein a controller fails and the first control and second controller can handle the fail over and maintain constant configuration of the drives. (Lines 65-68 of Column 3 and Lines 1-5 of Column 4).

c. Regarding the limitation of “starting a master switch timer that is less than a system timeout period if the first adaptor is the master after detecting the error, wherein

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an error recovery procedure in the system including the first adaptor would be initiated after the system timeout period has expired,” Powers discloses a system with a timeout counter for the I/O controller. (Lines 11-14 of Column 7). Once a timeout has occurred, a system failure is indicated and recovery proceeds. (Lines 24-30 of Column 7).

d. Regarding the limitation of “initiating an operation to designate another adaptor in the storage network as the master if the first adaptor is the master in response to detecting an expiration of one started I/O delay timer,” Powers discloses a system with wherein in response to the timeout, a secondary controller takes over as the primary and secondary controller. This is called BOTH STATES by the art. (Lines 65-67 of Column 7 and Line 1 of Column 8).

4. Regarding claim 2, Powers discloses a system wherein a timeout value times out. (Lines 24-27 of Column 7).

5. Regarding claim 3, Powers discloses a system only the controller with the fault shuts down for the fault recovery. (Lines 14-17 of Column 5).

6. Regarding claim 4, Power discloses a system wherein the controller that fails shuts down. It would be inherent that the controller would have to be restarted in order to be brought back online. (Lines 14-17 of Column 5).

7. Regarding claim 7:

e. Regarding the limitation of “initiating a monitoring state to monitor I/O requests transmitted through a second adaptor, in response to detecting the error” Powers discloses a system wherein a controller fails and the first control and second controller can handle

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the fail over and maintain constant configuration of the drives. (Lines 13-21 of Column 2).

f. Regarding the limitations of “starting an I/O delay timer that is less than the system timeout period in response to receiving an I/O request and send a reset request to the first adaptor in response to detecting an expiration of one started I/O delay timer,” Powers discloses a system with a timeout counter for the I/O controller. (Lines 11-14 of Column 7). Once a timeout has occurred, a system failure is indicated and recovery proceeds. (Lines 24-30 of Column 7).

8. Regarding claim 9, Powers discloses a system that can start a timeout period after an error detection (Lines 11-14 of Column 7) and releases a controller for the memory device for which it controlled upon the timeout period being reached. (Lines 24-32 of Column 7).

9. Regarding claim 12, Powers discloses system wherein the controller can suffer a complete failure, which results in total lack of communication with the memory devices. (Lines 23-27 of Column 2).

10. Regarding claim 13, Powers discloses a system wherein the secondary controller is a failure for the primary controller. (Lines 30-34 of Column 2).

11. Regarding claim 16, Power discloses a system wherein the memory devices are shown connected in a loop structure between the two controllers. (See Figure 1, Items 18A, 18B, 18M with 14A and 14B).

12. Regarding claim 18, Powers discloses system wherein the controller can suffer a complete failure, which results in total lack of communication with the memory devices. (Lines 23-27 of Column 2).

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13. Regarding claim 19:

g. Regarding the limitation of “a second adaptor capable of communicating on the storage network,” Powers discloses a system with a second controller. (Lines 66-67 of Column 1 and Lines 1-5 of Column 2).

h. Regarding the limitation of “detecting an error in a system including a first adaptor, wherein the first adaptor is capable of communicating on the storage network after the error is detected,” Powers discloses a system with a plurality of memory devices and components for controlling data flow with failure handling. (Lines 50-55 of Column 1).

i. Regarding the limitation of “determining whether the first adaptor is designated a master of the storage network after the error is,” Powers discloses a system wherein a controller fails and the first control and second controller can handle the fail over and maintain constant configuration of the drives. (Lines 65-68 of Column 3 and Lines 1-5 of Column 4).

j. Regarding the limitation of “starting a master switch timer that is less than a system timeout period if the first adaptor is the master after detecting the error, wherein an error recovery procedure in the system including the first adaptor would be initiated after the system timeout period has expired,” Powers discloses a system with a timeout counter for the I/O controller. (Lines 11-14 of Column 7). Once a timeout has occurred, a system failure is indicated and recovery proceeds. (Lines 24-30 of Column 7).

k. Regarding the limitation of “initiating an operation to designate another adaptor in the storage network as the master if the first adaptor is the master in response to detecting

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an expiration of one started I/O delay timer,” Powers discloses a system with wherein in response to the timeout, a secondary controller takes over as the primary and secondary controller. This is called BOTH STATES by the art. (Lines 65-67 of Column 7 and Line 1 of Column 8).

14. Regarding claim 20, Powers discloses a system wherein a timeout value times out. (Lines 24-27 of Column 7).

15. Regarding claim 21, Powers discloses a system only the controller with the fault shuts down for the fault recovery. (Lines 14-17 of Column 5).

16. Regarding claim 22, Power discloses a system wherein the controller that fails shuts down. It would be inherent that the controller would have to be restarted in order to be brought back online. (Lines 14-17 of Column 5).

17. Regarding claim 25:

l. Regarding the limitation of “initiating a monitoring state to monitor I/O requests transmitted through a second adaptor, in response to detecting the error” Powers discloses a system wherein a controller fails and the first control and second controller can handle the fail over and maintain constant configuration of the drives. (Lines 13-21 of Column 2).

m. Regarding the limitations of “starting an I/O delay timer that is less than the system timeout period in response to receiving an I/O request and send a reset request to the first adaptor in response to detecting an expiration of one started I/O delay timer,” Powers discloses a system with a timeout counter for the I/O controller. (Lines 11-14 of

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Column 7). Once a timeout has occurred, a system failure is indicated and recovery proceeds. (Lines 24-30 of Column 7).

18. Regarding claim 27, Powers discloses a system that can start a timeout period after an error detection (Lines 11-14 of Column 7) and releases a controller for the memory device for which it controlled upon the timeout period being reached. (Lines 24-32 of Column 7).

19. Regarding claim 30, Powers discloses system wherein the controller can suffer a complete failure, which results in total lack of communication with the memory devices. (Lines 23-27 of Column 2).

20. Regarding claim 31, Powers discloses a system wherein the secondary controller is a failure for the primary controller. (Lines 30-34 of Column 2).

21. Regarding claim 34, Power discloses a system wherein the memory devices are shown connected in a loop structure between the two controllers. (See Figure 1, Items 18A, 18B, 18M with 14A and 14B).

22. Regarding claim 36, Powers discloses system wherein the controller can suffer a complete failure, which results in total lack of communication with the memory devices. (Lines 23-27 of Column 2).

23. Regarding claim 37:

n. Regarding the limitation of “detecting an error in a system including a first adaptor, wherein the first adaptor is capable of communicating on the storage network after the error is detected,” Powers discloses a system with a plurality of memory devices and components for controlling data flow with failure handling. (Lines 50-55 of Column 1).

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- o. Regarding the limitation of “determining whether the first adaptor is designated a master of the storage network after the error is,” Powers discloses a system wherein a controller fails and the first control and second controller can handle the fail over and maintain constant configuration of the drives. (Lines 65-68 of Column 3 and Lines 1-5 of Column 4).
- p. Regarding the limitation of “starting a master switch timer that is less than a system timeout period if the first adaptor is the master after detecting the error, wherein an error recovery procedure in the system including the first adaptor would be initiated after the system timeout period has expired,” Powers discloses a system with a timeout counter for the I/O controller. (Lines 11-14 of Column 7). Once a timeout has occurred, a system failure is indicated and recovery proceeds. (Lines 24-30 of Column 7).
- q. Regarding the limitation of “initiating an operation to designate another adaptor in the storage network as the master if the first adaptor is the master in response to detecting an expiration of one started I/O delay timer,” Powers discloses a system with wherein in response to the timeout, a secondary controller takes over as the primary and secondary controller. This is called BOTH STATES by the art. (Lines 65-67 of Column 7 and Line 1 of Column 8).
24. Regarding claim 38, Powers discloses a system wherein a timeout value times out. (Lines 24-27 of Column 7).
25. Regarding claim 39, Powers discloses a system only the controller with the fault shuts down for the fault recovery. (Lines 14-17 of Column 5).

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26. Regarding claim 40, Power discloses a system wherein the controller that fails shuts down. It would be inherent that the controller would have to be restarted in order to be brought back online. (Lines 14-17 of Column 5).

27. Regarding claim 43:

r. Regarding the limitation of “initiating a monitoring state to monitor I/O requests transmitted through a second adaptor, in response to detecting the error” Powers discloses a system wherein a controller fails and the first control and second controller can handle the fail over and maintain constant configuration of the drives. (Lines 13-21 of Column 2).

s. Regarding the limitations of “starting an I/O delay timer that is less than the system timeout period in response to receiving an I/O request and send a reset request to the first adaptor in response to detecting an expiration of one started I/O delay timer,” Powers discloses a system with a timeout counter for the I/O controller. (Lines 11-14 of Column 7). Once a timeout has occurred, a system failure is indicated and recovery proceeds. (Lines 24-30 of Column 7).

28. Regarding claim 45, Powers discloses a system that can start a timeout period after an error detection (Lines 11-14 of Column 7) and releases a controller for the memory device for which it controlled upon the timeout period being reached. (Lines 24-32 of Column 7).

29. Regarding claim 48, Powers discloses system wherein the controller can suffer a complete failure, which results in total lack of communication with the memory devices. (Lines 23-27 of Column 2).

30. Regarding claim 49, Powers discloses a system wherein the secondary controller is a failure for the primary controller. (Lines 30-34 of Column 2).

31. Regarding claim 52, Power discloses a system wherein the memory devices are shown connected in a loop structure between the two controllers. (See Figure 1, Items 18A, 18B, 18M with 14A and 14B).

32. Regarding claim 54, Powers discloses system wherein the controller can suffer a complete failure, which results in total lack of communication with the memory devices. (Lines 23-27 of Column 2).

Claim Rejections - 35 USC § 101

33. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 37 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. A “computer readable medium containing computer executable instructions to perform the steps of...” is the proper claim language for an “article of manufacture including code for processing...” as claimed in claim 37.

Claim Objections

34. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest

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numbered claims previously presented (whether entered or not). Claim number 24 is dependant from claim 24. The examiner believes claim 24 should be dependant from claim 23. The examiner would like clarification from the applicant regarding the claim dependency.

Allowable Subject Matter

35. Claims 5-6, 8, 10-11, 14-15, 17, 23-24, 26, 28-29, 32-33, 35, 41-42, 44, 46-47, 50-51, and 53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura**.

- The examiner can normally be reached on **Mon-Fri: 7:30-5:00, every other Friday off**. The examiner can be reached at: **703-305-7762**.

37. If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, **Rob Beausoliel**.

- The supervisor can be reached on **703-305-9713**.

38. The fax phone numbers for the organization where this application or proceeding is assigned are:

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- **703-872-9306 for all patent related correspondence by FAX.**

39. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov/>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

40. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **703-305-3900**.

41. Responses should be mailed to:


- **Commissioner of Patents and Trademarks**

P.O. Box 1450

Alexandria, VA 22313-1450

Tim Bonura
Examiner
Art Unit 2114

tmb
July 29, 2004


ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100